LightWise Camera Series

LW-5-S-1394 FireWire™
Smart Digital Imaging Module

LW-5-S-1394-C – Color
Available in Color Only.

Specification and Users Guide
Revision 2.1a

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Table of Contents:

1 LW-5-S-1394 Introduction and Specification Overview
- 1.1 Product Description
- 1.2 Key Specifications
- 1.3 5 MP Image Sensor
- 1.4 Programming and User Configuration Options
- 1.5 Automatic Gain and Offset Correction
- 1.6 On-Board Image Buffer
- 1.7 Digital Panning & Scaling (Zoom)
- 1.8 JPEG Compression
- 1.9 Simplified Block Diagram

2 External Signals and Connectors
- 2.1 External Trigger Modes
- 2.2 External Connectors

3 Programming Guide
- 3.1 Top Level Memory Map
- 3.2 Register Detail

4 Mechanical Information
- 4.1 Lens Mount
- 4.2 Tripod Connection
- 4.3 Digital Imaging Module Dimensions
- 4.4 Module Components
- 4.5 Operating Conditions

5 Firmware and FPGA Upgrade Process

Appendix A: Color Image Processing Pipeline
Appendix B: IIDC 1394-based Digital Camera Specification

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Section 1: LW-5-S-1394-C Introduction and Specification Overview

1.1 Product Description

The ISG LW-5-S-1394-C 'Smart' Digital Imaging Module provides a High Resolution area imaging solution with outstanding flexibility. The low cost and ease of integration into existing systems make it an excellent solution for a wide variety of applications. The interfaces to the Imager are industry standard to provide ease of integration into target systems. Applications include:

Automated Inspection Systems
2D Bar Code Reading
Machine Vision Systems
Encoding and Positioning
Parcel Scanning
Programmable Smart Camera Applications
Smart Surveillance
Security and Homeland Defense.

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1.2 Key Specifications

- Resolution: 2592 x 1944 Pixels
- Color only Available
- Synchronous Shutter (Rolling) with advanced Trigger/Strobe capability
- Data Rate:
    - Up to 15 Frames / second full resolution (2592 x 1944)
    - Up to 23 Frames / second partial frame (3 Mp – 2048 x 1536)
    - Up to 35 Frames / second partial frame (2 Mp – 1600 x 1200)
    - Up to 48 Frames / second partial frame (1.3 Mp – 1280 x 1024)
    - Up to 70 Frames / second VGA
    - Scalable frame rate as a function of Region of Interest
    - **Please note that 1394a bus bandwidth limitation may limit sustained video throughput rates.**
- Data Resolution: On-Chip 12 bit A to D
- Dynamic Range >70dB Signal to Noise Ration > 38dB
- On-Board FPN Correction
- On-Board Multiple Frame Image Buffer (SRAM)
    - For up to 3 Color Images
- Optional JPEG and M-JPEG – not possible with current board set but ISG can offer this with additional engineering contract for new board set.
- Digital Panning with Flexible Region of Interest
- Standard FireWire™ (1394a) Interface (see TM note, page 23)
    - Fully compliant to IEEE-1394a IIDC DCAM Specification Version 1.3
- Single 12V Supply via FireWire
- Compact Form Factor
- User Programmable Exposure Timing and Frame Rate
- Built-In Test Pattern

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- I/O for Triggers and Synchronization Flexibility
- On-Board FPGA for User-Configurability
    - Customized Image Processing Capability
    - Customized Programmable I/O
- High Quality Digital Panning and Zoom Capabilities.

1.2.1 ISG Color Image Processing Pipeline

The LW-5-S-1394-C Color Imaging Module utilizes the ISG Hardware Image Processing Pipeline implemented in a Xilinx™ FPGA. All color processing parameters are fully programmable by the user. Appendix B describes the image path.

1.3 5 MP CMOS Image Sensor

The module utilizes a 5 MP CMOS image sensor. Please contact ISG for Sensor details if needed. 2592 x 1944.

1.4 Programming and User Configuration Options

The LW-5-S-1394-C offers several levels of programmability and user configurability. These include:

- Full Parameter Control, Set-Up and Operation Control via the **ISG Graphical User Interface Software**. This software is included with each unit.

- Full Parameter Control, Set-Up and Operation Control via **direct access of the module's register set**. Section 3 is the programmer's reference for this mode of operation.

- **Customization of on-board FPGA**. The on-board FPGA can be customized to include 'Smart' Camera functionality, such as specialized image processing, data feature

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extraction, custom dynamic range mapping, JPEG Compression , etc. This method can also be used to configure the external I/O signals for custom functionality. Imaging Solutions Group is available for consulting with customers to design or enable custom configurations via the on-board FPGA. Contact sales@isgchips.com for information.

1.5 Automatic Gain and Offset Correction

The LW-5-S-1394-C will provide on-board FPN correction through gain and offset compensation. The FPGA algorithms in conjunction with an on-board dual 8-bit DAC perform automatic offset correction and semiautomatic gain corrections. These functions can be selected and activated by the provided ISG Graphical User Interface (GUI) software, or can be accessed directly via register programming.

1.6 On-Board Image Buffer

The LW-5-S-1394-C provides on-board image buffering for up to one raw or 5 JPEG frame color or three frames raw monochrome full resolution 2592 x 1944. Combined with the module's flexible trigger modes, this image buffer enables capturing a sequence of frames at the maximum frame rate of the sensor, then transferring the frames at any available 1394 bandwidth.

1.7 Digital Panning Scaling (Zoom)

The LW-5-S-1394-C camera provides full frame rate smooth digital panning. This allows a region of interest of any size to be swept through the entire active viewing area via host computer control. A very high quality digital scaling function is also implemented for Zoom feature capability.

1.8 JPEG Compression

The current board set cannot offer this option. However, ISG can add this option, with associated NRE.

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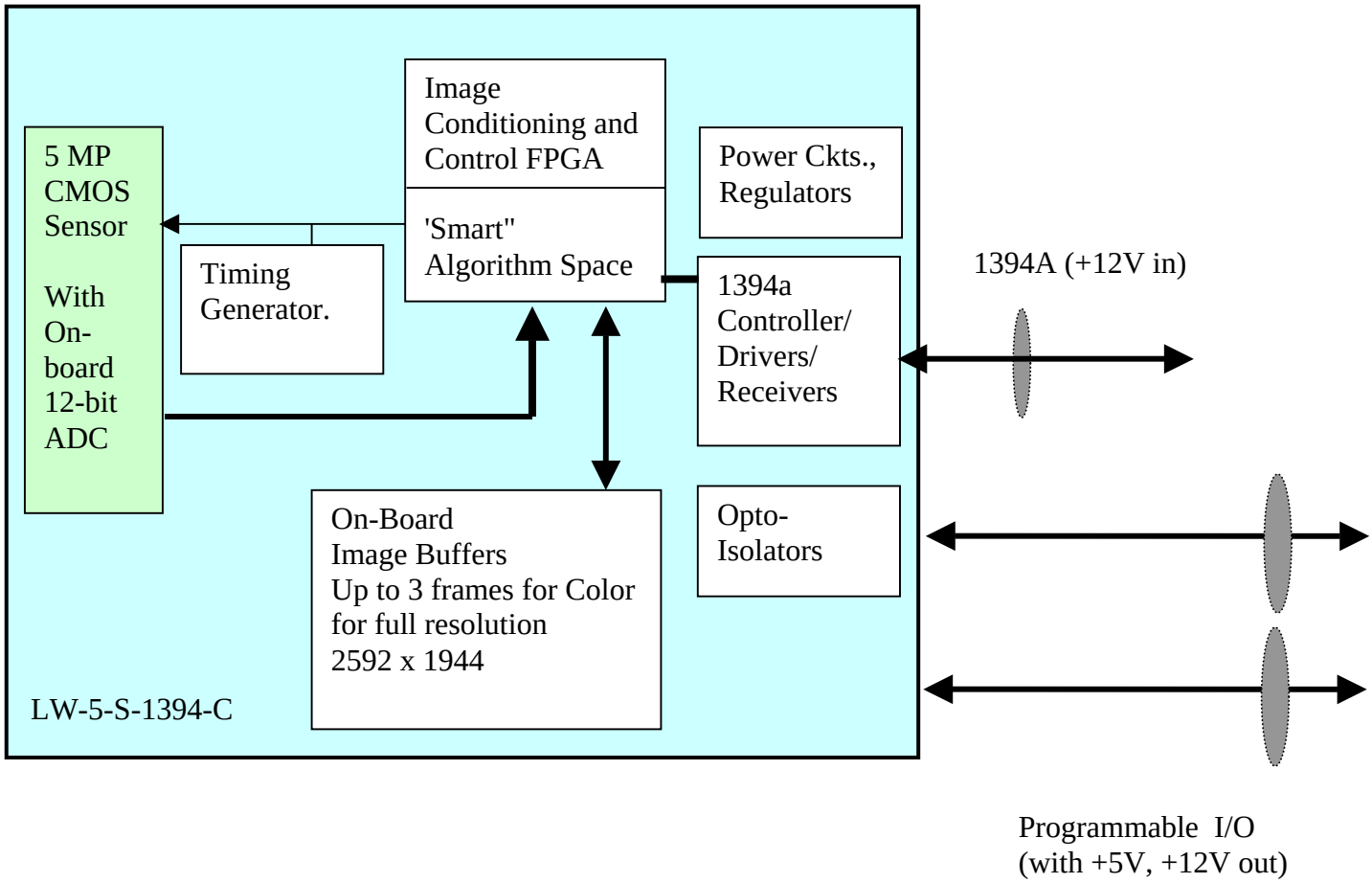
1.9 Simplified Block Diagram



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Section 2: Connectors and Trigger Modes

Section 2.1:

ISG Camera Module Triggering Description

The ISG camera module provides a variety of triggering modes and flexibility using features internal to the FPGA controller as well as the sensor. For a more detailed description of the registers referenced in this document see the Programmers Reference manual.

Register Description:

Trigger Delay – A 16 bit value used to delay the start of integration from the active edge of the input trigger. This value can be programmed in steps of 20.83us to a maximum value of 1.37s.

Strobe Advance – This 8 bit register is used to apply the strobe signal a programmed amount of time before the start of sensor integration to allow for illumination turn on time. This value can be programmed in steps of 5.21us to a maximum value of 1.33ms. Note: The trigger delay must be greater then the strobe advance.

Strobe Delay – This 16 bit register is used to delay the strobe signal a programmed amount of time after the start of sensor integration. This delay is intended for use with flash illumination devices. This value can be programmed in steps of .65us to a maximum value of 42.7ms. Note: The strobe delay must not exceed the integration time of the sensor. If a value is programmed for Strobe Advance the Strobe Delay value will be ignored.

Retrigger Delay – The 16 bit value in this register is used to program the time between integration intervals when in Retrigger Mode. This value can be programmed in steps of 5.2us to a maximum value of 341ms.

Strobe Duration - This register is used to program the duration of the strobe pulse when strobe duration mode is enabled. This value can be programmed in steps of 5.2us to a maximum value of 341ms. Note: The strobe output will go inactive at the end of sensor integration no mater what the strobe duration is set to.

Trigger and Strobe Description:

The input trigger sense can be active low or high. A software trigger is also available to the programming interface (Host Mode) as well as a trigger status bit. The strobe output is intended to control an illumination system and can be selected to be active low or high as well as always high or always low. The diagrams on the following pages show the trigger as active low and the strobe as active high.

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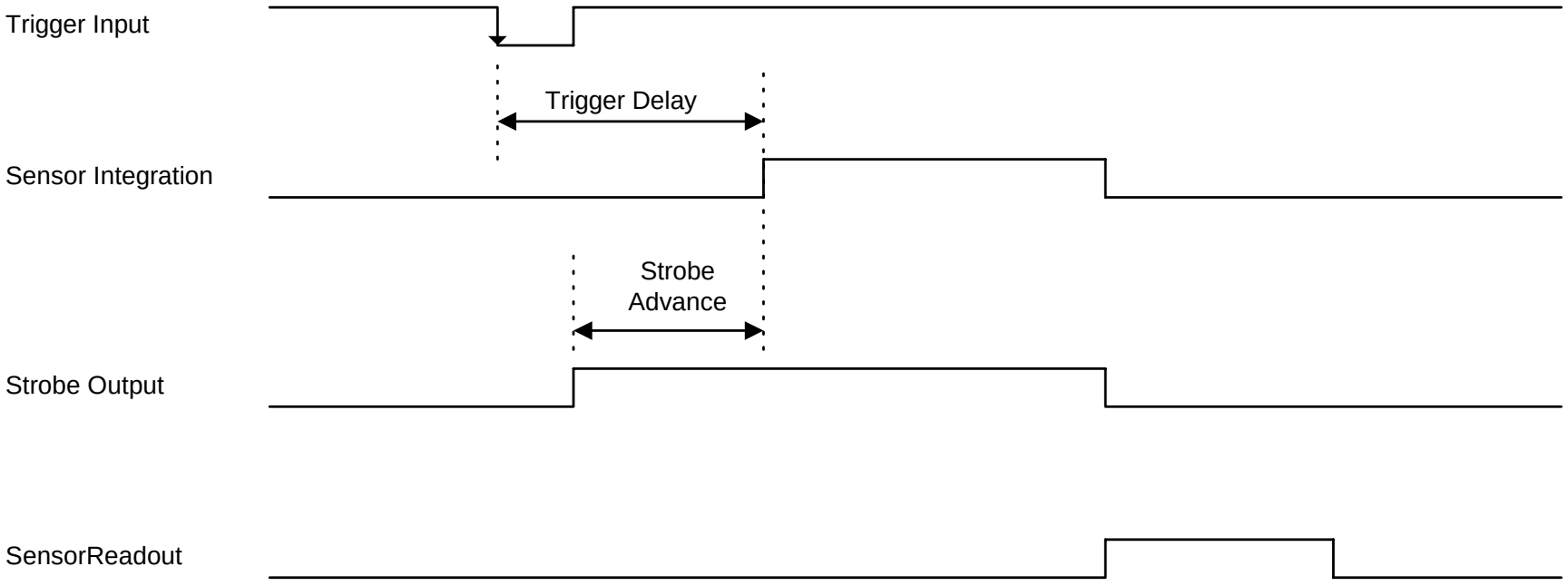
Trigger Mode A = IIDC Trigger Mode 0
Strobe Advance Shown



Note: In this mode the integratin time is determined by a register setting.

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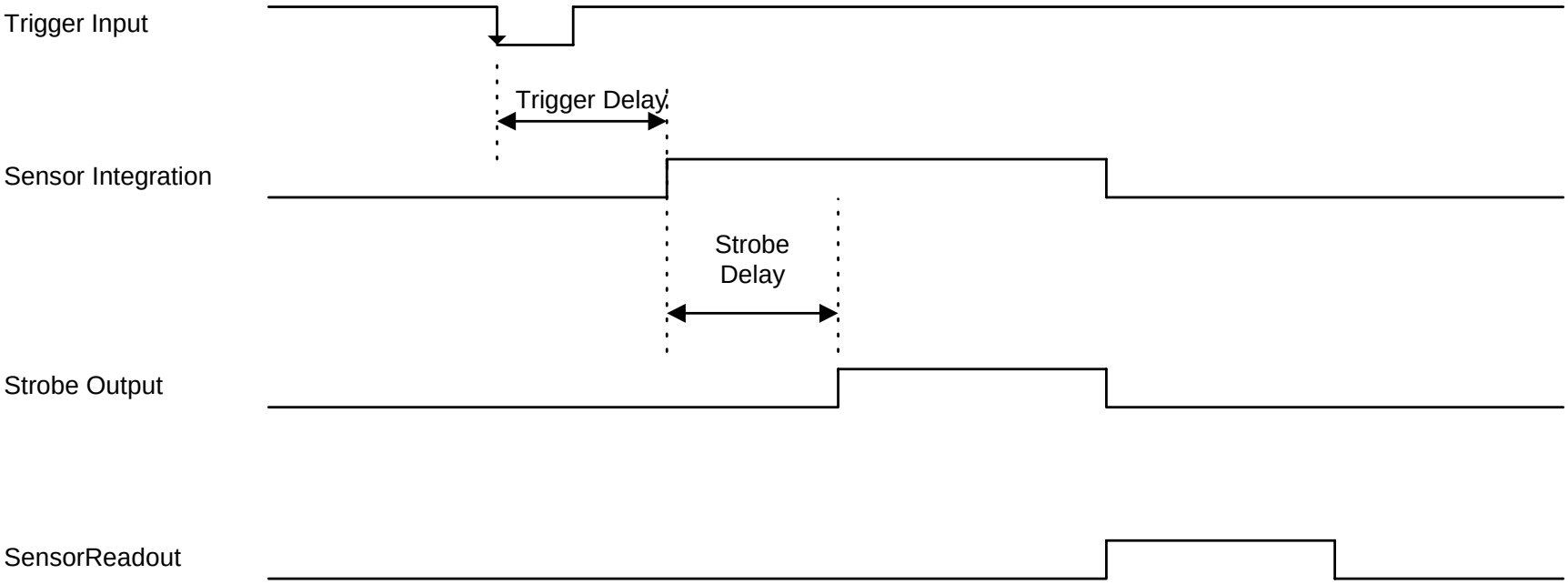
Trigger Mode A = IIDC Trigger Mode 0
Strobe Delay Shown



Note: In this mode the integratin time is determined by a register setting.

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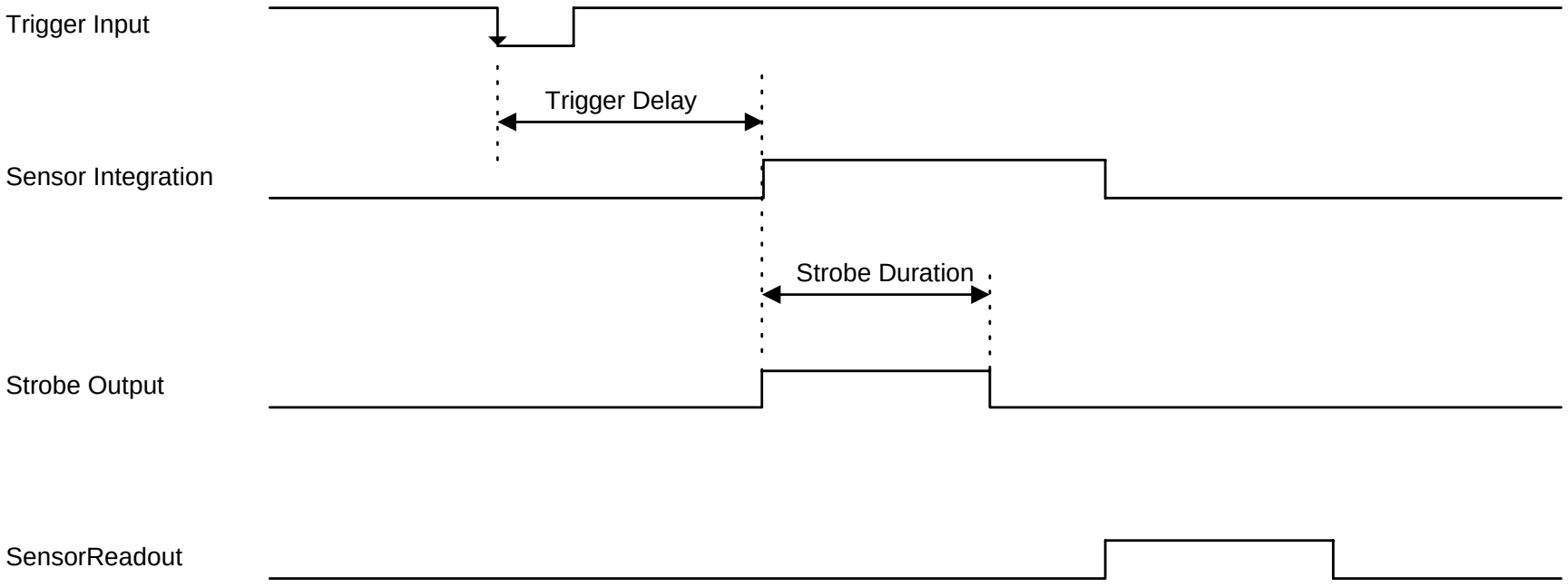
Trigger Mode A = IIDC Trigger Mode 0
Strobe Duration Shown



Note: In this mode the strobe duration is determined by the strobe duration registor. Also, the Strobe Duration mode bit must be enabled.

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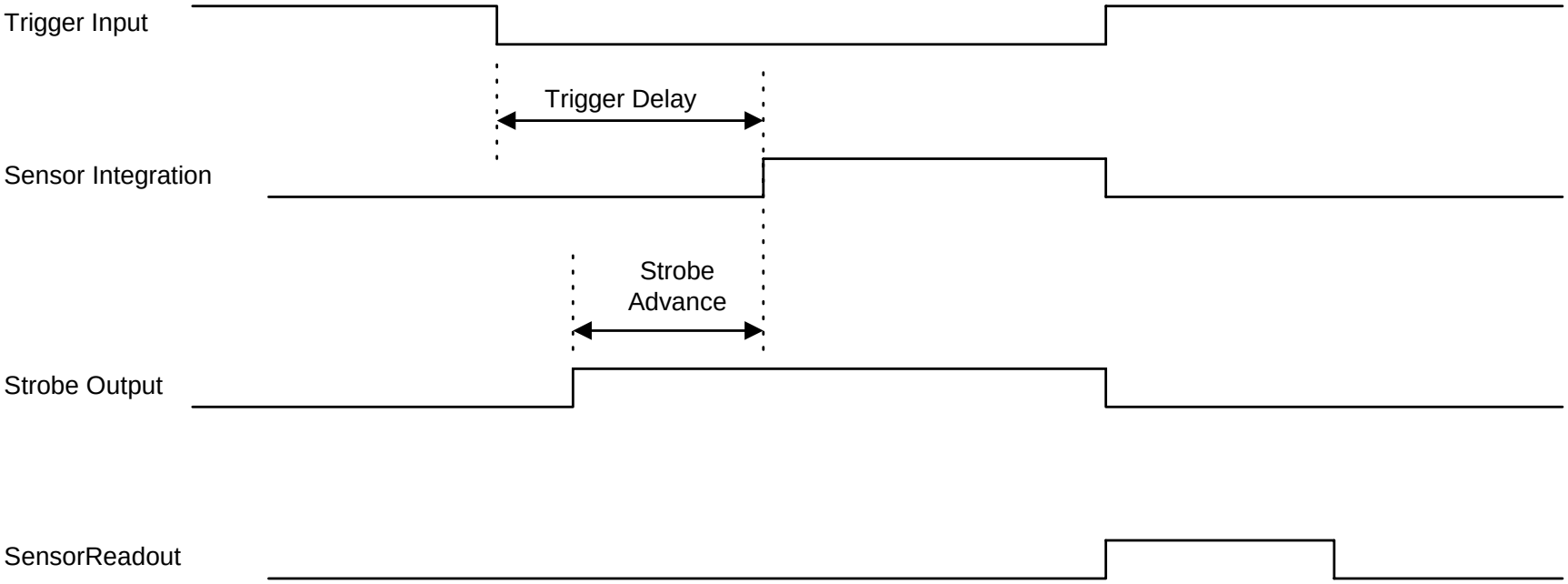
Trigger Mode B = IIDC Trigger Mode 1



Note: In this mode the integratin time is determined by the trigger duration.

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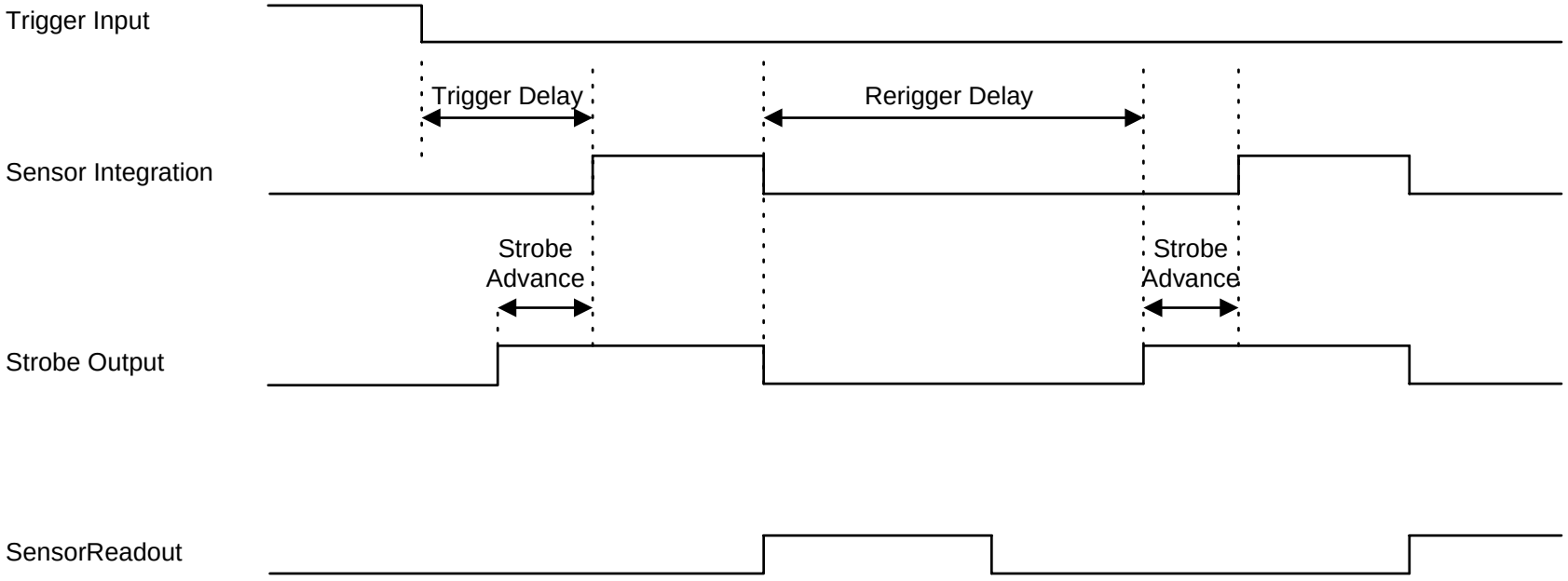
Trigger Mode C



Note: In this mode the integratin time is determined by a register setting.

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2.2 External Connectors

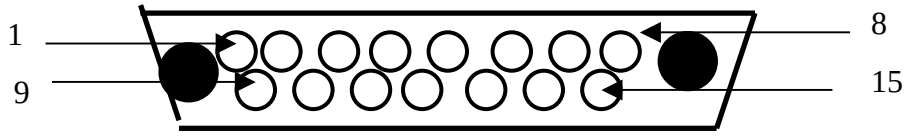
2.2.1 Firewire™ Connector: This interface is based on the industry standard 1394a specification. Two connectors are provided to allow camera daisy chaining.

2.2.2 15-position D-SUB I/O Connector:

- Connector part number: Molex part number 83612-9020
- Thumb Screw part number: Molex MDSM – 9PE-Z10-VR25

- Recommended Cable: Molex CA 83422-9014

Pin	Function	Input/Output Type
1	Trigger +	Optoisolated Input
2	Trigger -	Optoisolated Input
3	GND	
4	DC Input (Optional)	Power Input
5	Strobe	Open Collector Output
6	Programmable PWM	Open Collector Output
7	GND	
8	DC Input (Optional)	Power Input
9	RS422 Trigger +	Diff. TTL Input
10	RS422 Trigger -	Diff. TTL Input
11	DC +5V Output	Power Output
12	Programmable Output +	Optoisolated Output
13	Programmable Output -	Optoisolated Output
14	Reserved	
15	GND	



15-pin Micro-D **EXT IO Connector, Front View**

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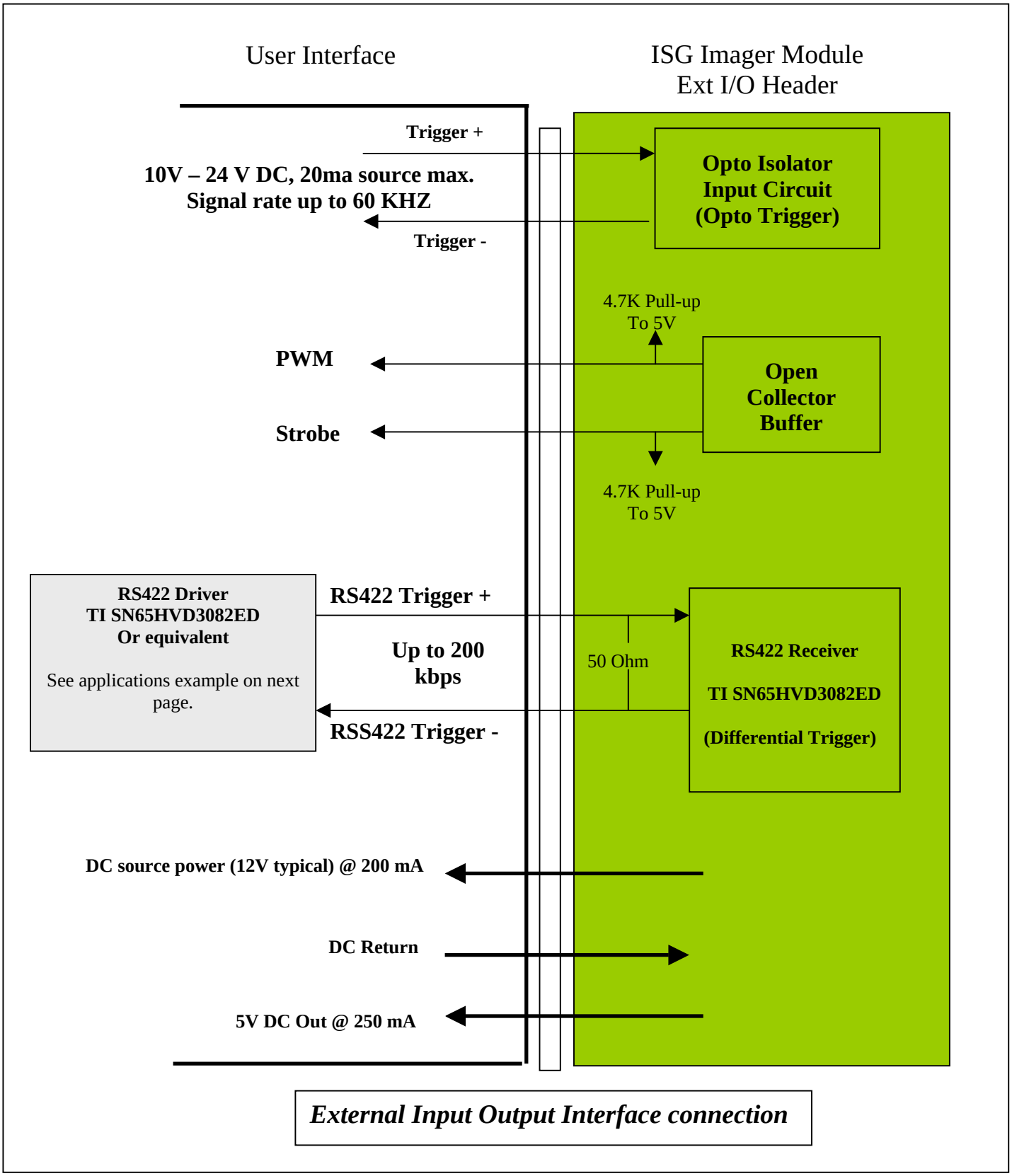

External Input Output Interface connection

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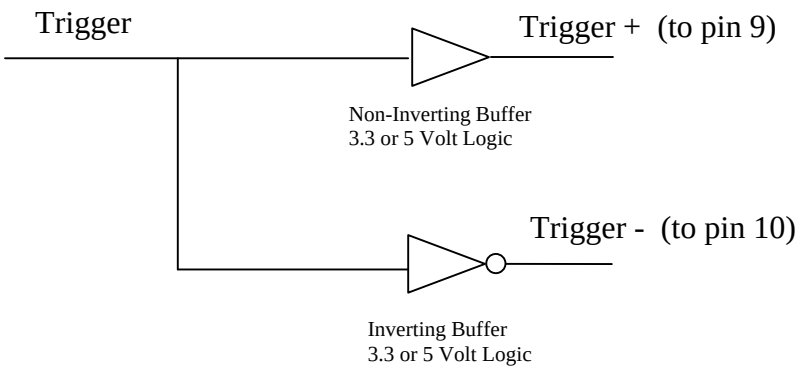
Applications Example: Using The RS422 Trigger Input

1) Preferred Method – RS422 Driver

The optimal way to utilize this input to trigger the camera is to drive the RS422 Receiver in the camera with the corresponding driver device. The recommended driver is TI part number SN65HVD3082ED. This method provides a balanced, robust differential input.

2) Alternate Method - Driving the RS422 Trigger Input with Standard 3.3 or 5 Volt CMOS/TTL Logic

Standard digital logic can be used to simulate a differential signal and trigger the camera using the RS422 input. This can be accomplished by generating a 3.3 or 5 Volt logic signal for RS422 Trigger +, and providing a logically inverted output of this signal for RS422 Trigger -. The following diagram illustrates this approach:



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Section 3: Programming Guide

3.1 Top Level Memory Map: All addresses are offset from address 0x7000

Sensor Map	0x000 - 0x3ff	B12	

Sensor Interface

SICR	0x400	B15	Sensor Interface Control (Control Register1)
SISTAT	0x404		Sensor Interface Status
TRGDLY	0x408	U16	Trigger Delay
STRBDLY	0x40C	U16	Strobe Delay
RTGDLY	0x410	U16	Retrigger Delay
PWM	0x414	U8	PWM Duty Cycle
STRADV	0x418	U8	Strobe Advance
STRDUR	0x41C	U16	Strobe Duration
VVDLY	0x420	U4	Video Valid Delay
IBISCR	0x424	B10	Not Used
INTCNT0	0x428	U32	Not Used
INTCNT1	0x42C	U32	Not Used
INTCNT2	0x430	U32	Not Used
INTCNT3	0x434	U32	Not Used
PADCNT	0x43C	U32	Not Used
IBACCUM	0x440		Not Used
STATVAR	0x444	U5	Not Used
CLKCR	0x448	U5	Clock Divider/Control
SERRB	0x44C		Data from serial (delayed) read

Color Image Path or Mono Image Path Control

IPCR	0x800	B14	Image Path Control
IPSTAT	0x804	B2	Image Path Status
HISTCOLSTRT	0x808	U12	Histogram Window Column Start
HISTCOLWIDTH	0x80C	U12	Histogram Window Column Width
HISTROWSTRT	0x810	U11	Histogram Window Row Start
HISTROWDEPTH	0x814	U11	Histogram Window Row Depth
HISTCR	0x818	B4	Histogram Control
HISTADDR	0x81C	U5	Histogram Address
HISTDATA	0x820	U26	Histogram Data
DGAIN	0x824	U4.4	Digital Gain
LUTADDR	0x8B4	U10	Look Up Table Address
LUTDATA	0x8B8	U10	Look Up Table Data

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3.2 Register Detail

Note: Some data formats are given as (S/U # of integer bits. # of fractional bits). For example, S1.3 means the value can be either positive or negative with the first bit indicating the sign, one integer bit and three fractional bits. U0.8 means no sign bit (positive number), zero integer bits and eight fractional bits. Negative values must be programmed as 2's complement. A format of Bn means a binary format with n bits used.

Address : 400x0 (CNTL1)
Data format : B15
Default Value: 00h

15	14	13	12	11	10	9	8
Not used			OUTFMT[3:0]				LUTEN

7	6	5	4	3	2	1	0
IMRST	TRGSNS	VIDEN	HTRIG	STRBM[1:0]		TRIGM[1:0]	

TRIGM: Trigger Mode. These bits control the trigger source as well as trigger operation.
TRIGM[1:0] = 00 : Local Trigger, One Shot
TRIGM[1:0] = 01 : Local Trigger, Retriggerable
TRIGM[1:0] = 10 : Host Trigger, One Shot
TRIGM[1:0] = 11 : Host Trigger, Retriggerable

Local Trigger: Trigger is input directly to camera via external connector.
Host Trigger: Trigger is issued via 1394 interface.
One Shot: Edge on trigger input initiates one video frame.
Retriggerable: Repeats Frames as long as trigger input is active. Time between frames controlled by **RTGDLY** register.

When in one-shot mode, integration time can be controlled by the FPGA, the IBIS sensor or the trigger duration. The control for this is located in Control Register 2. The table below shows some possible modes and register settings using an external trigger.

Trigger Mode	TRIGM[1:0]	IBMODE[1:0] (Control Reg 2)
Trigger mode A (IIDC Trigger Mode 0)	00b	10b Use FPGA register to control integration time.
Trigger mode B (IIDC Trigger Mode 1)	00b	11b Use trigger duration to control integration time.
Trigger mode C	01b	01b Use sensor register to control integration time.

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STRBM : Strobe Mode. These bits control the functionality of the Strobe output to the illumination system.
STRBM[1:0] = 00 : Active high (Activated by trigger).
STRBM[1:0] = 01 : Active Low (Activated by trigger).
STRBM[1:0] = 10 : Always high (Not activated by trigger).
STRBM[1:0] = 11 : Always low (Not activated by trigger).

HTRIG : Host trigger bit. Asserted via 1394 interface.

VIDEN : Video Enable bit. This bit is set after imager is initialized.

TRGSNS: Trigger Sense

IMRST: Imager Reset, Controls the SS_RESET pin on IBIS Sensor

OUTFMT: Output Format. These bits control the output data format.
OUTFMT[3:0] = 0000 : 8 bit data output. (default)
OUTFMT[3:0] = 0001 : 10 bit data output in 16 bit field with LSB's padded with 0.
OUTFMT[3:0] = 0010 : 10 bit data output in 16 bit field with MSB's padded with 0.
OUTFMT[3:0] = 0100 : Test pattern Enable
OUTFMT[3:0] = 1000 : 10 bit data. No padding.

LUTEN: Look up Table Enable. Set this bit to '1' to enable 10 bit to 10 bit data mapping via programmable look up table. Reset this bit to '0' to bypass look up table.

Address : 0x404 (STAT)
Data format : B1
Default Value: 00h

7	6	5	4	3	2	1	0
not used							TSTAT

TSTAT : Trigger Status. This read only bit is high when local trigger is asserted.

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Address : 0x408 (TRGDLY)
Data format : U16
Default Value: 00h

15	14	13	12	11	10	9	8
TRGDLY(15:8)							

7	6	5	4	3	2	1	0
TRGDLY(7:0)							

TRGDLY : This 16 bit Value is used to program a delay from the time trigger is received to when strobe is activated. A delay between 0 and 1.37s in 20.83us steps can be achieved. The default value is 0.

Address : 0x40c (STBADV)
Data format : U16
Default Value: 00h

15	14	13	12	11	10	9	8
STBADV(15:8)							

7	6	5	4	3	2	1	0
STBADV(7:0)							

STBADV : This 8 bit Value is used to program the delay between the Strobe output (illumination) and tart of sensor integration. The default value is 0.

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Address : 0x410 (RTGDLY)
Data format : U16
Default Value: 00h

15	14	13	12	11	10	9	8
RTGDLY(15:8)							

7	6	5	4	3	2	1	0
RTGDLY(7:0)							

RTGDLY : This 16 bit Value is used to program the delay between video frames in continues trigger

Mode. A delay between 0 and 341ms in 5.21us steps can be achieved. The default value is 0.

Address : 0x414 (PWM)
Data format : U8
Default Value : 80h

7	6	5	4	3	2	1	0
PWM(7:0)							

PWM : PWM Duty Cycle. This register controls the duty cycle of the 13Khz PWM signal fed to the illumination system. FFh = 100%, 80h = 50%, 00h = .4%.

Address : 0x41c (VERREG)
Data format : B8
Default Value : 0Bh

7	6	5	4	3	2	1	0
VERREG(7:0)							

VERREG : The value in this register is used to identify the FPGA firmware revision.

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Address : 0x420 (VVDLY)
Data format : B4
Default Value : 02h

7	6	5	4	3	2	1	0
not used				VVDLY(3:0)			

VVDLY : Video Valid Delay. The value in this register is used to move the video relative to the video valid signal internal to the FPGA.

Address : 0x448 (CLKCR)
Data format : U5
Default Value: 0h

7	6	5	4	3	2	1	0
not used			INV	CLKDIV(3:0)			

INV: When this bit is set, the sensor clock is inverted.

CLKDIV : Clock Divider. The sensor base clock rate is 48Mhz for Micron and 48Mhz for IBIS. This value is R/W.

Address : 0x824 (DGAIN)
Data format : U4.4
Default Value : 10h

7	6	5	4	3	2	1	0
DGAIN(7:0)							

DGAIN : Digital Gain. The input video is multiplied by this value. The result is truncated to 1023. The range of DGAIN is 0 to 15.9375 in steps of 1/16. This value is R/W.

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Address : 0x818 (HCS)
Data format : B2

7	6	5	4	3	2	1	0
not used						STAT	LOCK

LOCK : Histogram lock out control. This bit is R/W
0 = Histogram values are updated at the end of each frame.
1 = Histogram values are NOT updated at the end of each frame. Lock out updates to read the Histogram results. Setting this bit also clears the status bit.

STAT : Status bit is set at the end of a frame when the histogram is available. The status bit is cleared by setting the LOCK bit.

Address : 0x2xx (HIST0L)
Data format : U21

23	22	21	20	19	18	17	16
not used			HIST0[20:16]				

15	14	13	12	11	10	9	8
HIST0[15:8]							

7	6	5	4	3	2	1	0
HIST0[7:0]							

HIST0 : Histogram Bin 0. This register is Read Only.

Address : 0x2d0 – 0x2e8 (HIST1 – HIST7)

Histogram Bins 1 thru 7 follow the same format as Histogram Bin 0.

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Address : 0x8b4 (LUTAD)
Data format : U10

15	14	13	12	11	10	9	8
not used						LUTAD[9:8]	

7	6	5	4	3	2	1	0
LUTAD[7:0]							

LUTAD : LUT Address Register. Reads and writes from the LUT data register use the value in this register as the address into the LUT. Reads/Writes to the data register causes the value in this register to be incremented by 1. Hence, the LUTs can be loaded by successive writes to the data register. This register is R/W.

Address : 0x8b8 (LUTDATA)
Data format : 2x U10

15	14	13	12	11	10	9	8
not used						LUTADATA [9:8]	

7	6	5	4	3	2	1	0
LUTDATA-E[7:0]							

LUTDATA : LUT Address Register. Values written to this register are written to the LUT at the location specified by LUTAD. Reads/Writes to this register cause the LUTAD register to be incremented. This register is R/W.

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Section 4: Mechanical Information

4.1 Lens Mount

A Case-Mount **CS** type (1.0” diameters with 12.5 mm spacing between the surface of the sensor and top of the lens-mount) lens mount is provided for both system configurations.

C-Type Lenses: A five mm extender will change the CS to C-Type lens mount with 17.5 mm Back Focal Length.

F-Type Lenses: Using the Cannon 50mm F-type FD series + the Canon "C-type to F-type" adapter will covert the camera to F-type with 39.9 mm Back Focal Length.

4.2 Tripod Connection

A standard female tripod connection is provided at the bottom of the Digital Imaging Module and the Evaluation platform

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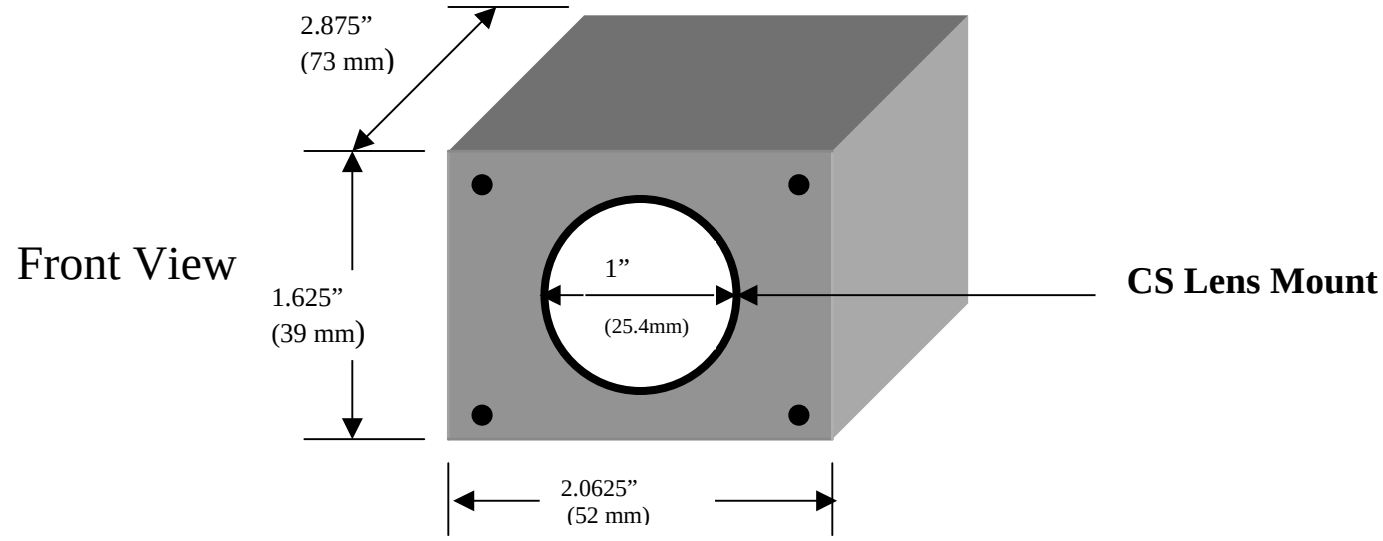
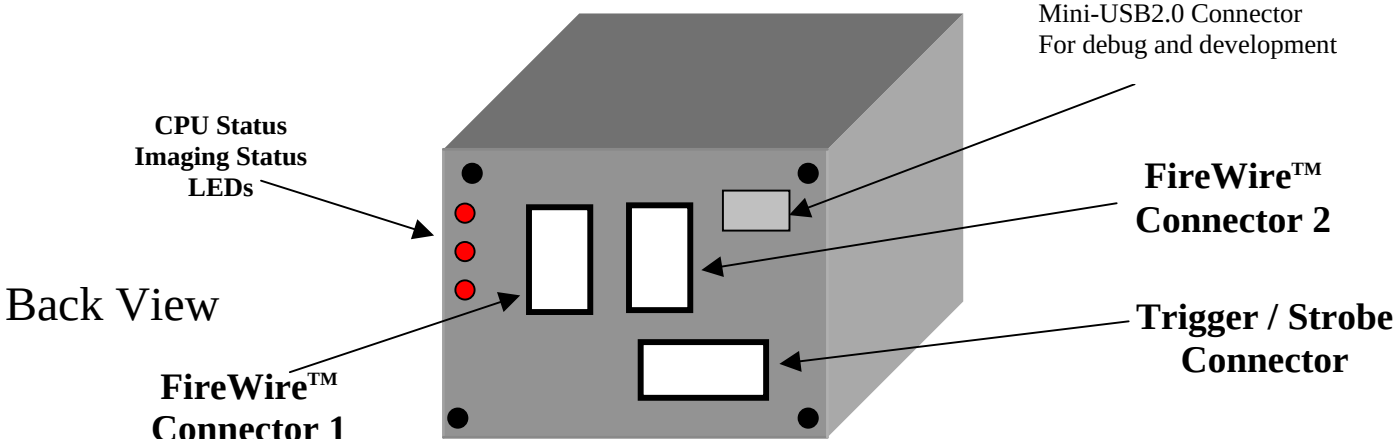
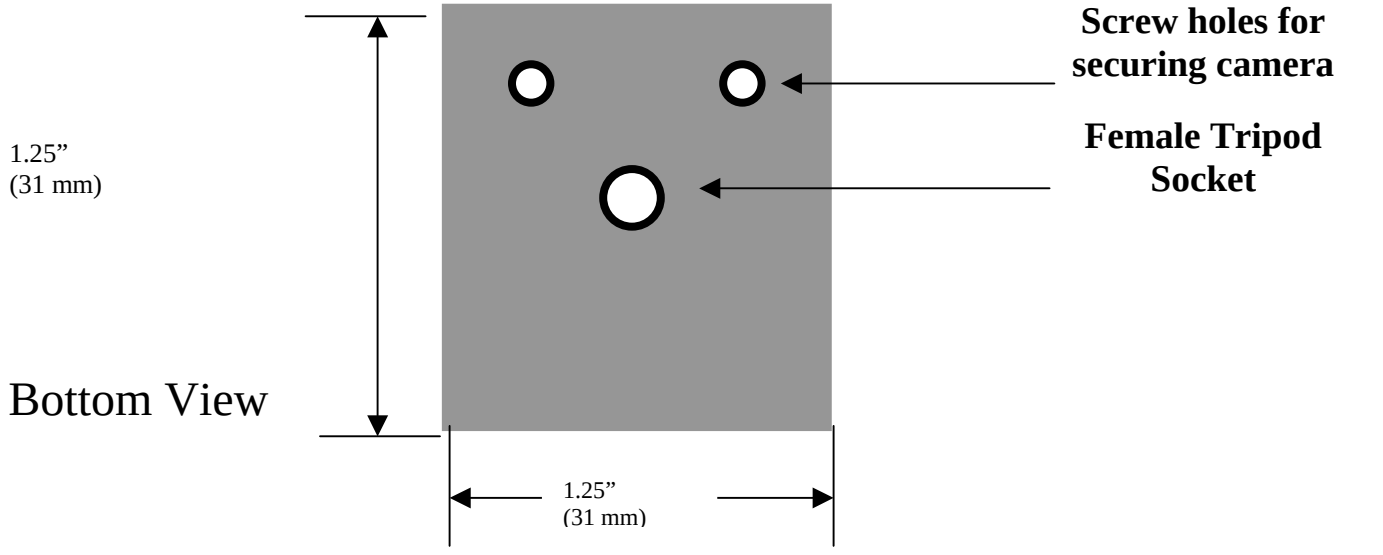
4.3 LW-5-S-1394-C Digital Imaging Module Dimensions







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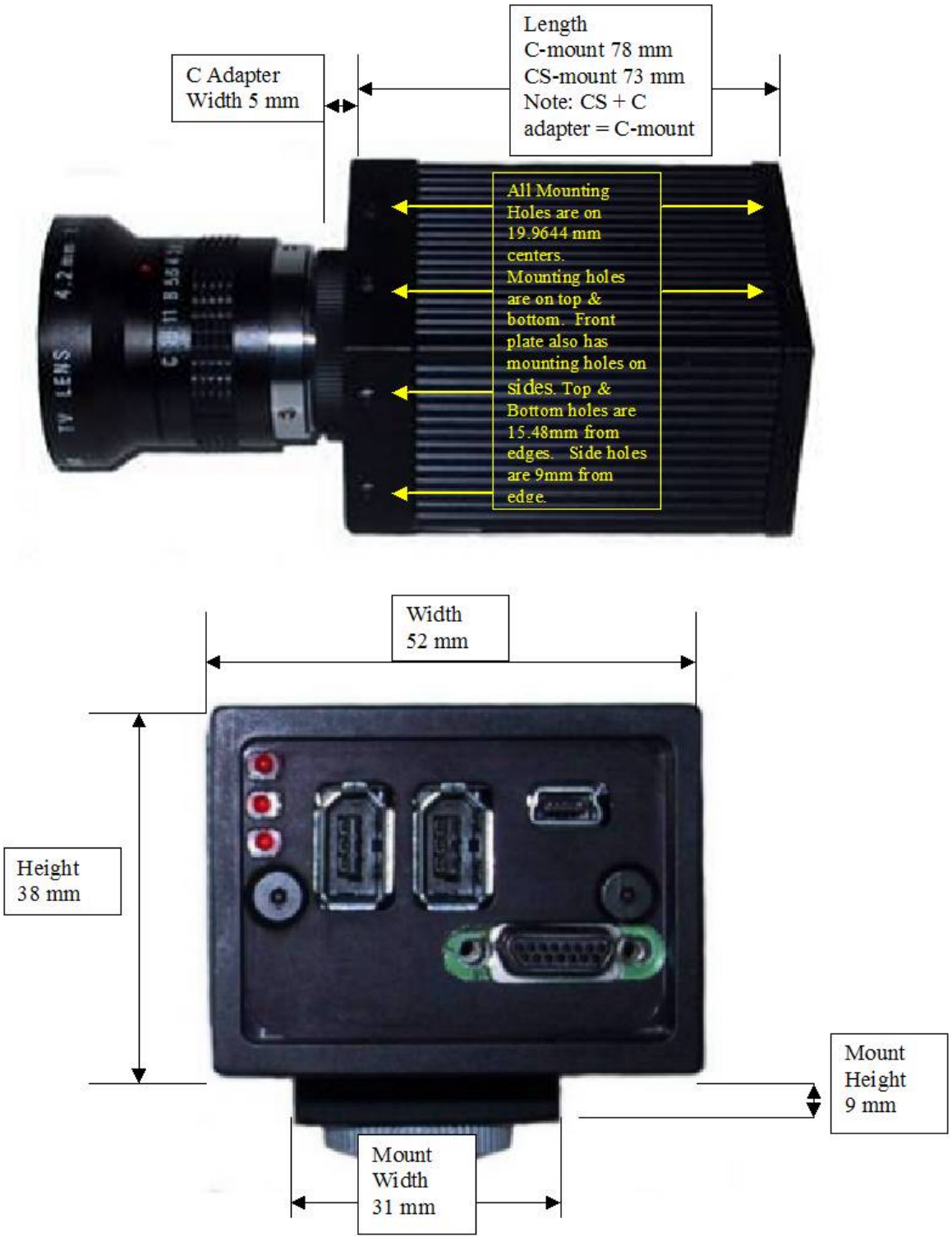

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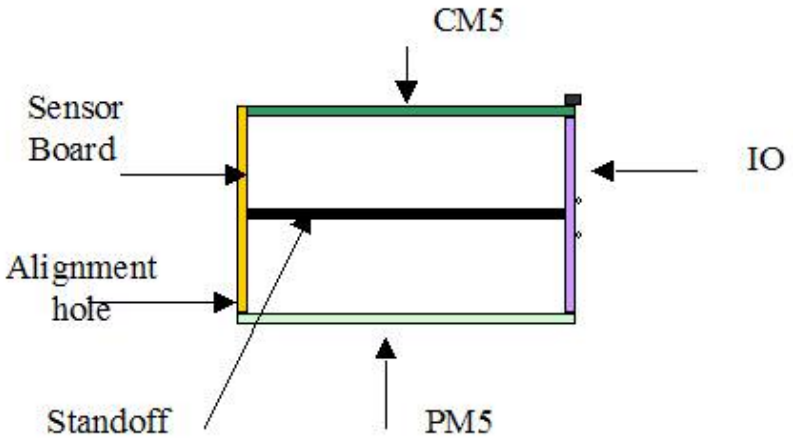
4.4 Module Components:

The ISG LW-5-S-1394-C Digital Imaging Module hardware design is partitioned into four separate boards: 1) Sensor, 2) Controller, 3) Power Management and 4) I/O boards. These boards are SMT type 2 (double sides) and are connected to each others as shown below:

The module electronics consists of 4 boards: Sensor, Controller (CM5), Power Management Board (PM5) and the IO board.



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4.5 Operating Conditions

Measured Average Power Consumption via 1394 cable:
12V, 250 ma rms / 3.0W

Ambient Operating Temperature Range:
-10 to 45 C

FCC and CE Qualification: In progress.
Test results available upon request.

Vibration and Shock Testing: In progress.
Target specification: 7G rms (10Hz to 2000Hz) Random, Shock 70G. Test results available upon request.

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5.0 ISG Firmware + FPGA Upgrade Process

This process will use the ISG Camera Control GUI application software on the host PC, to update firmware and/or FPGA code on the ISG 1394 camera. The camera's firmware/FPGA code is loaded through the 1394 interface using the ISG GUI.

A customer wishing to do a firmware or FPGA upgrade should perform the following steps:

1) Extract, and copy the firmware/FPGA binary data files to a directory on your host PC. The files are named isgcpu_ccxx_xxxx.bin for updating the camera firmware, and isgfpga_ccxx_xxxx.bin for updating the camera hardware (i.e. FPGA device code). The ccxx field represents the camera type, and the xxxx field will hold the version number.

2) To upgrade the firmware on the camera, start by running the ISG Lightwise GUI. Note that the ISG supplied driver for the camera must be installed in order to use the ISG GUI. It is recommended that the camera viewer window be closed before continuing.

3) Click on the "Camera Control Dialog" button on the ISG GUI.

4) Select the "Camera Setup" tab from the Camera Control Dialog page. The Camera Setup page can be used to update either the firmware or the FPGA code of the camera, or both.

5) Use the browse button (labeled "…") to search for and select either the isgcpu or isgfpga binary file defined in step 1 above, depending on which part of the camera you are updating.

6) To begin the actual download procedure, click on the "Download to CPU" or "Download to HW" button as appropriate. A popup box will ask if you are sure that you want to continue the process.

7) Confirm that you are sure you want to proceed with the upgrade by answering, "yes" within the confirmation popup dialog. Once confirmed, insure that this process is not interrupted (i.e. maintain 1394 cable connection). The progress bar will show the status of the update. Note that an FPGA update will take a few minutes to complete. The process is completed once the dialog states "Done" on the download button. At this point, the camera is upgraded with new firmware/FPGA code.

8) Exit the GUI. Power cycle the camera by disconnecting and reconnecting the 1394 cable to allow the new code to be executed.

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9). After the camera is connected, you can right click in the top toolbar of the GUI and select “about isg camera system” to read the new version numbers.

Trade Mark Note:

FireWire™ is a registered trademark of Apple Inc

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APPENDIX A: ISG Color Image Processing Pipeline